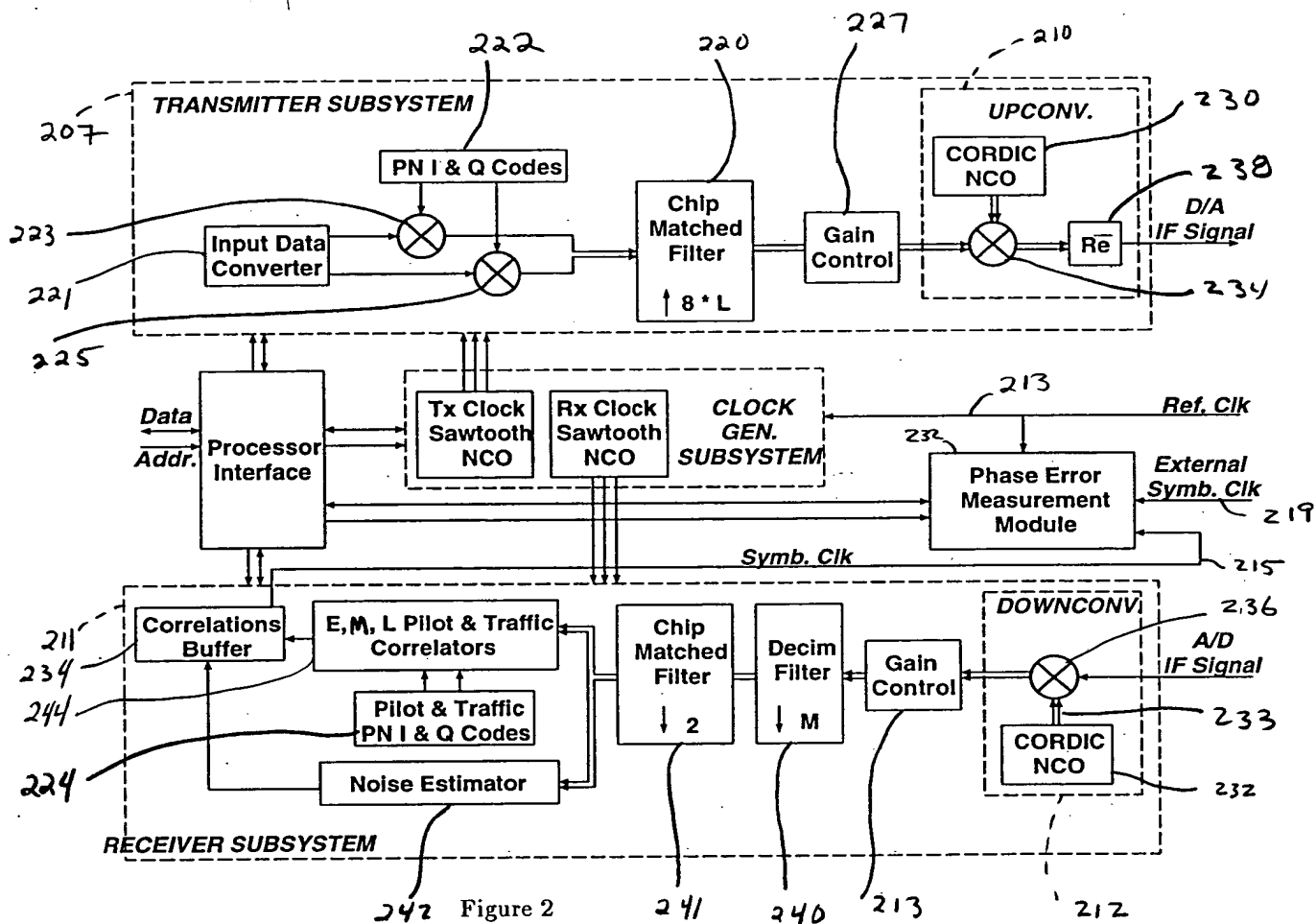


FIG. 1

005207 925960



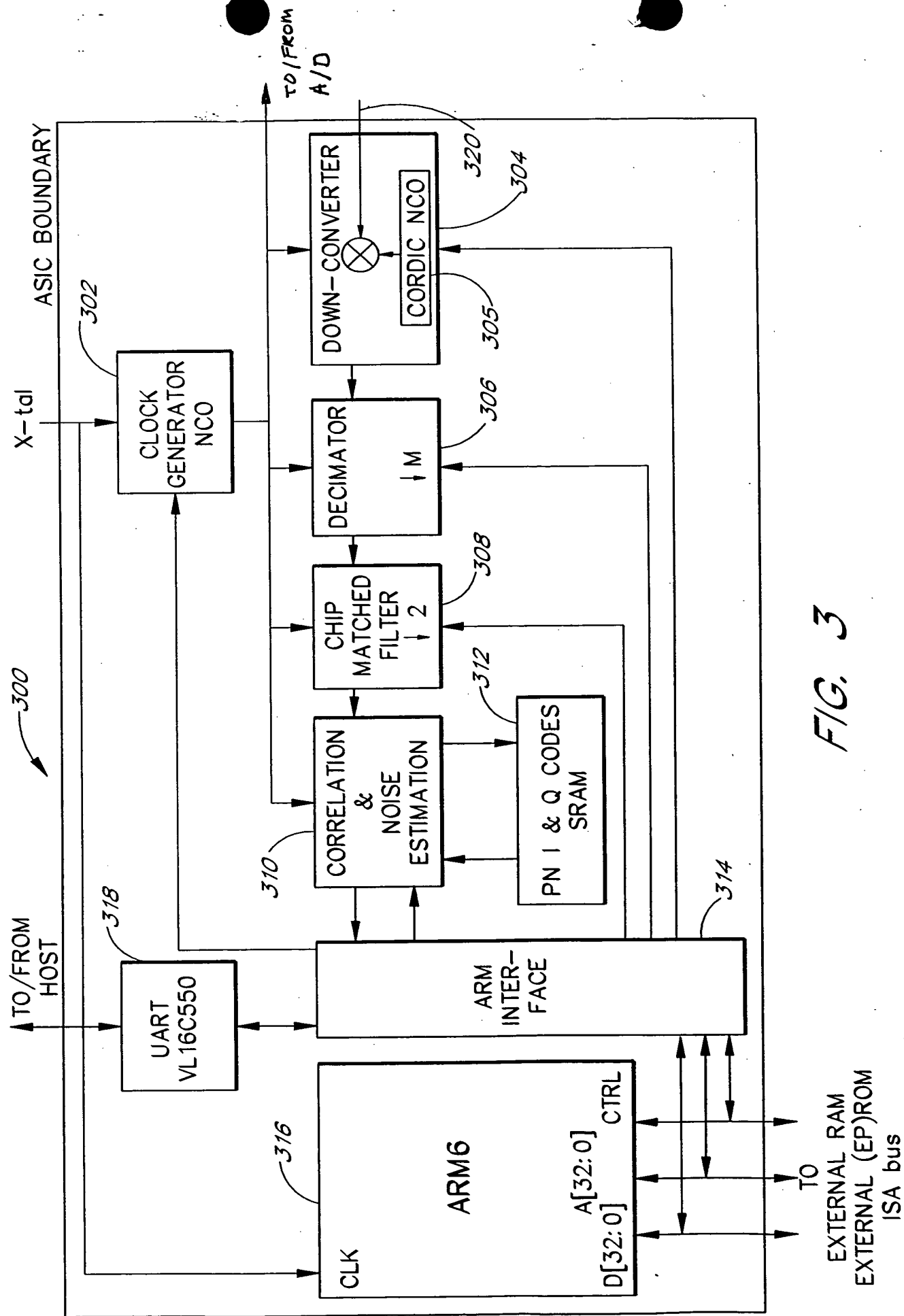


FIG. 3

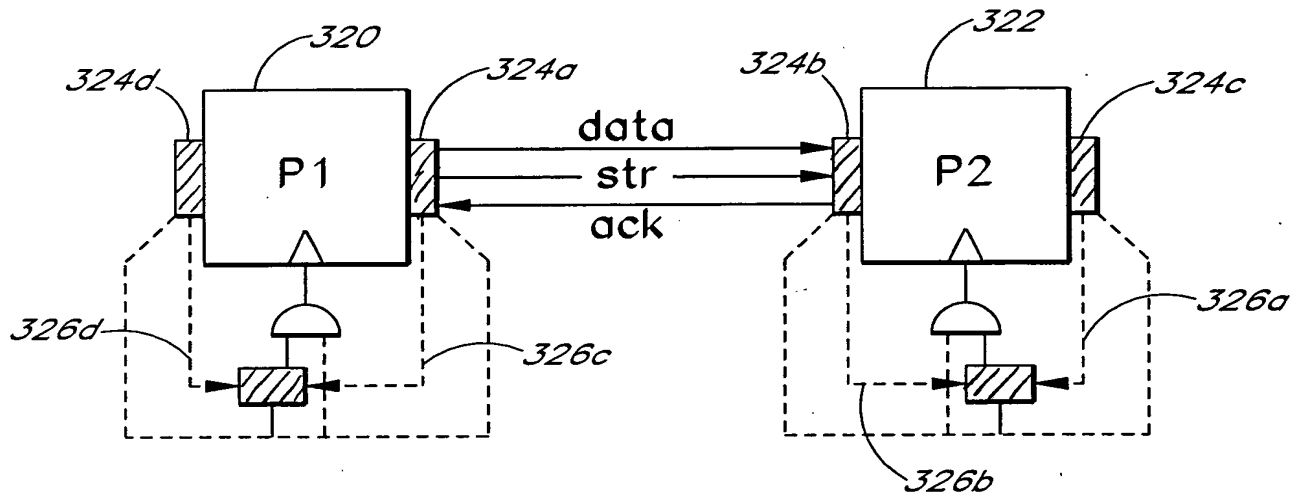


FIG. 4

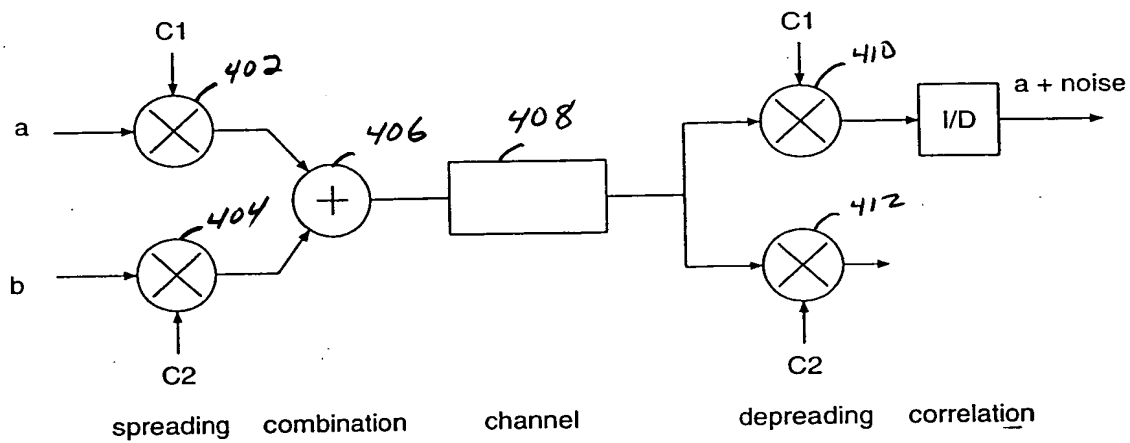


Figure 5:

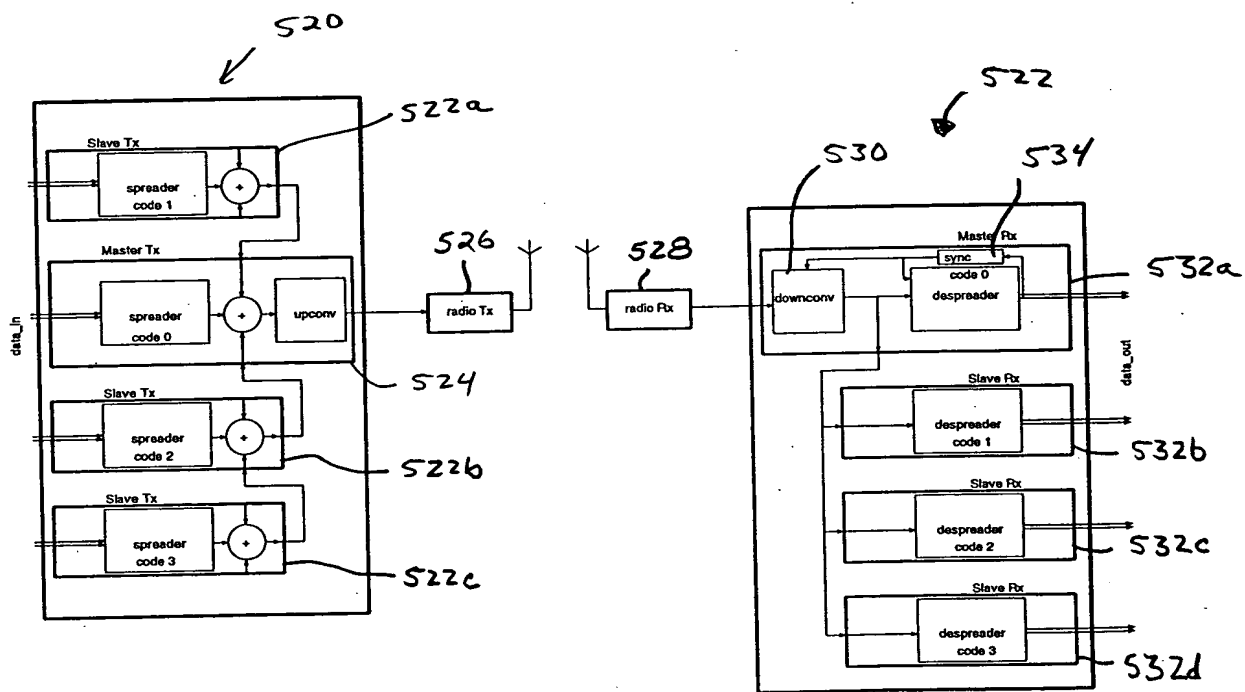


Figure 6

005207" 9E896960

500 →

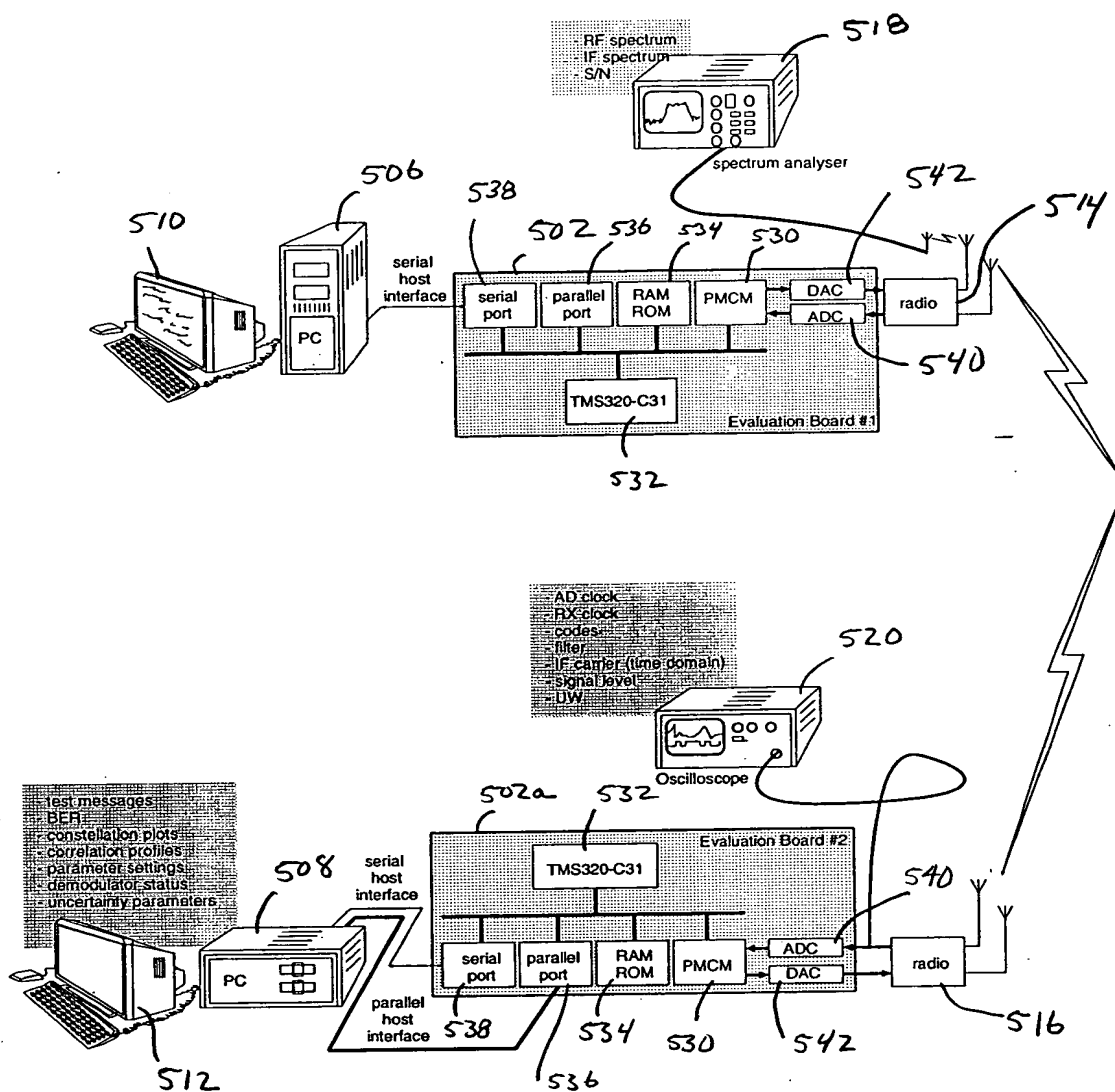


Figure 7

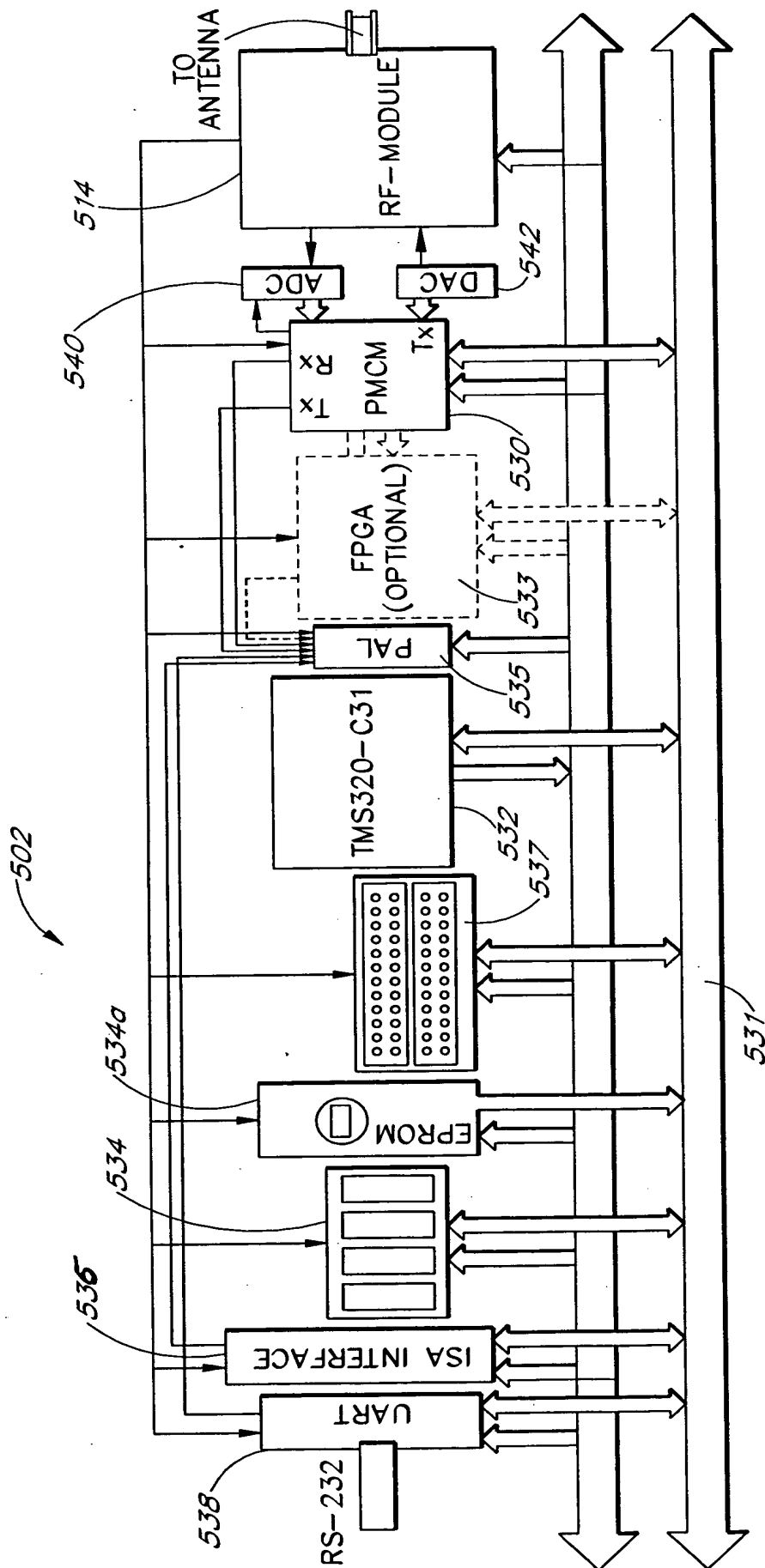


FIG. 8

The diagram illustrates the test setup for the TMS320C31 evaluation board. A PC (labeled 506) is connected to the board via a serial host interface and a parallel host interface. The board contains a TMS320C31 processor, serial port, parallel port, RAM ROM, PMCM, ADC, and DAC. The DAC output passes through an attenuator (labeled 502b) before being connected to an oscilloscope (labeled 520). The oscilloscope is also connected to a spectrum analyser (labeled 518). The spectrum analyser displays the IF spectrum and S/N. The test setup is configured to measure the signal level and uncertainty parameters.

Test Setup Components and Connections:

- PC (506):** Connected to the Evaluation Board via serial and parallel host interfaces. It provides test messages, BER, constellation plots, correlation profiles, parameter settings, demodulator status, and uncertainty parameters.
- Evaluation Board:** Contains the TMS320C31 processor, serial port, parallel port, RAM ROM, PMCM, ADC, and DAC.
- Oscilloscope (520):** Connected to the DAC output (via an attenuator) and the spectrum analyser. It displays the signal waveform.
- Spectrum Analyser (518):** Connected to the oscilloscope. It displays the IF spectrum and S/N.

Test Parameters and Settings:

- AD clock
- RX clock
- codes
- filter
- IF carrier (time domain)
- signal level
- UW

Figure 9:

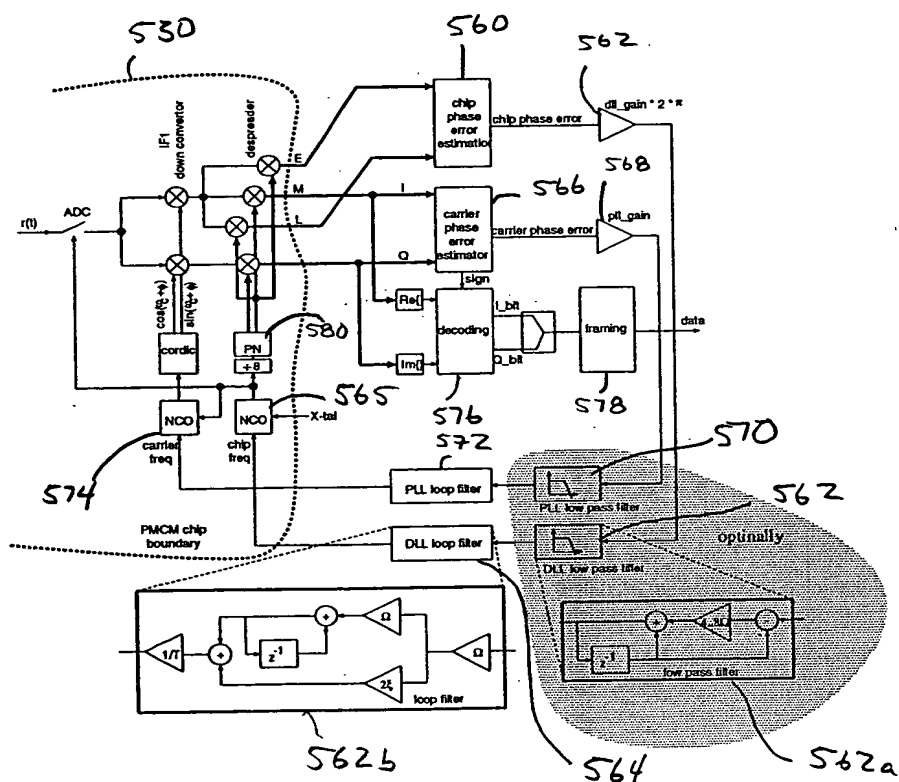


Figure 10

005207" 9E896960

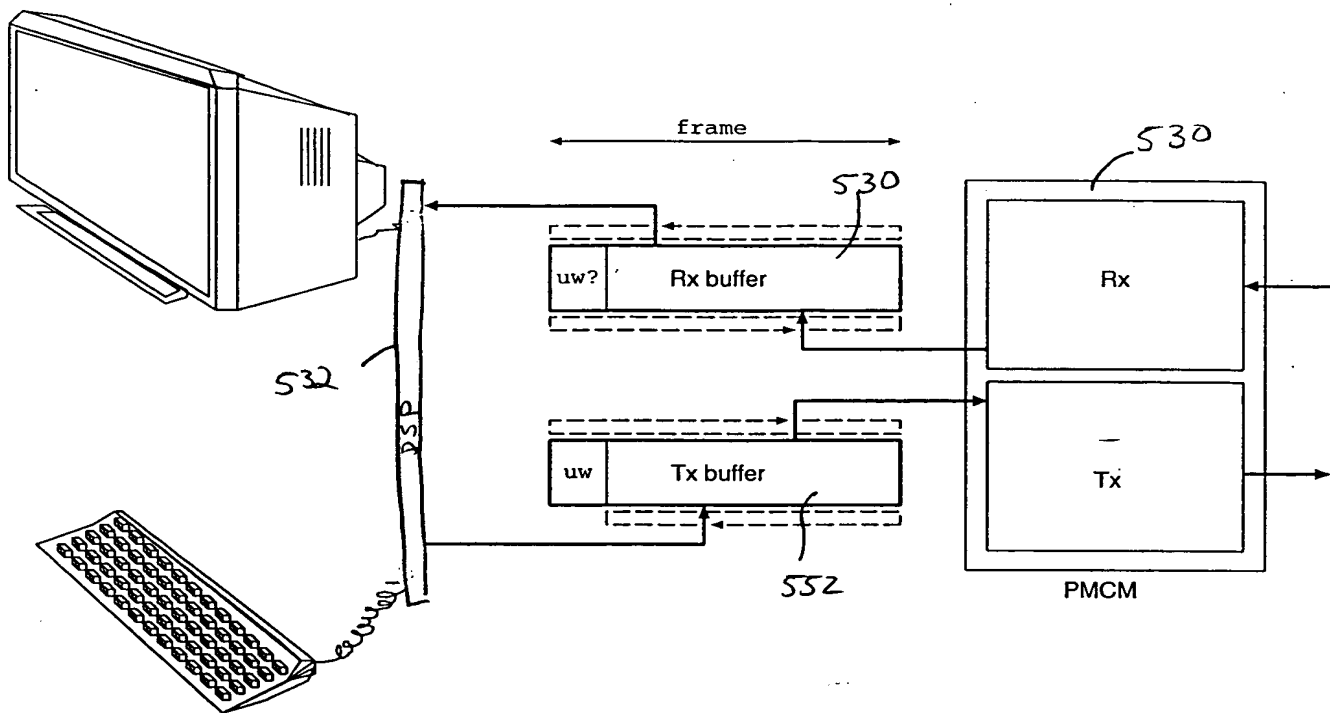


Figure 11

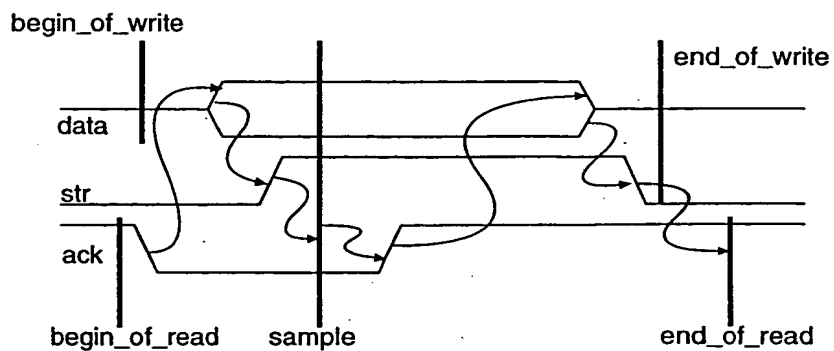


Figure 12

00696836 " 102500

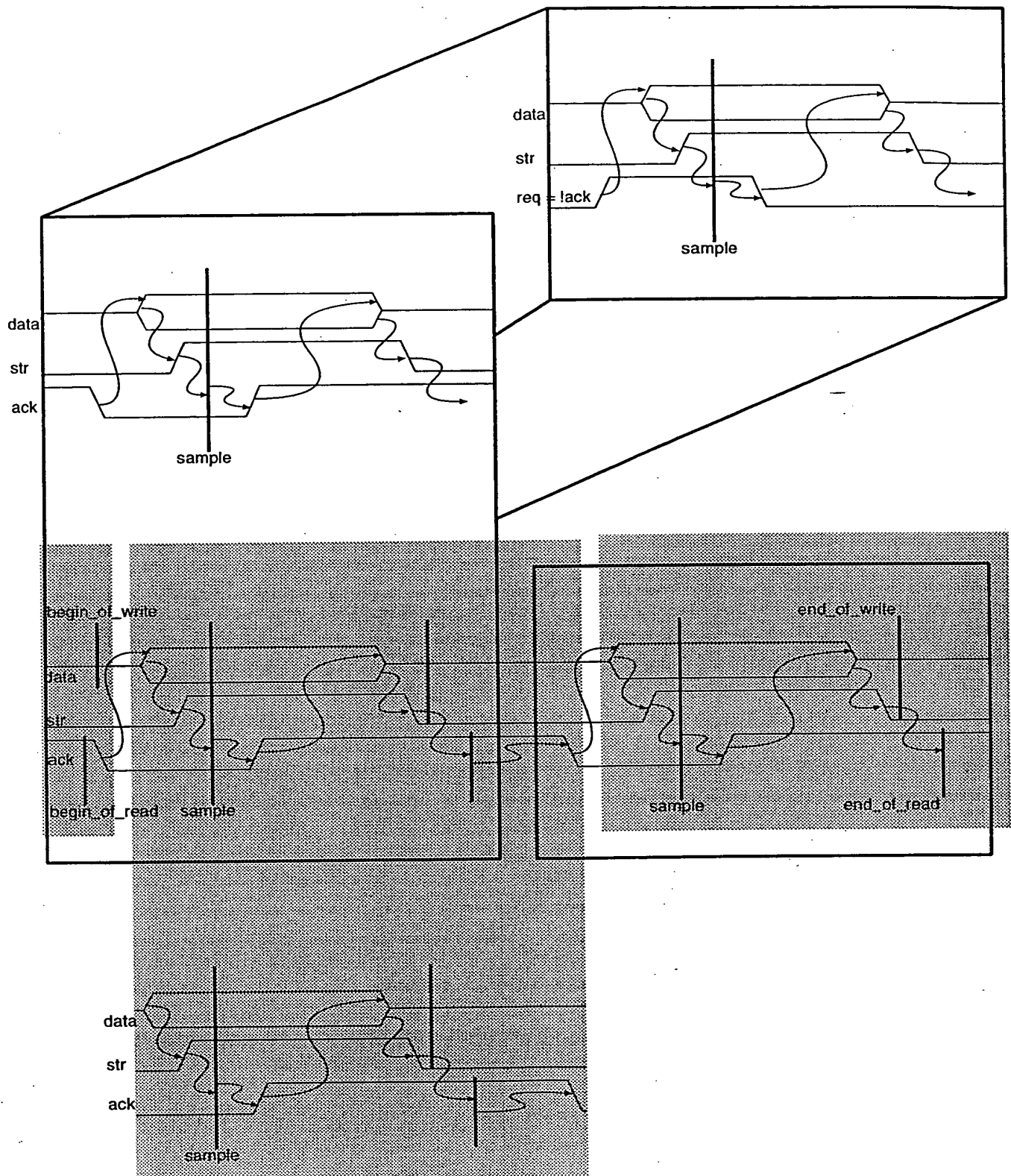


Figure 13.

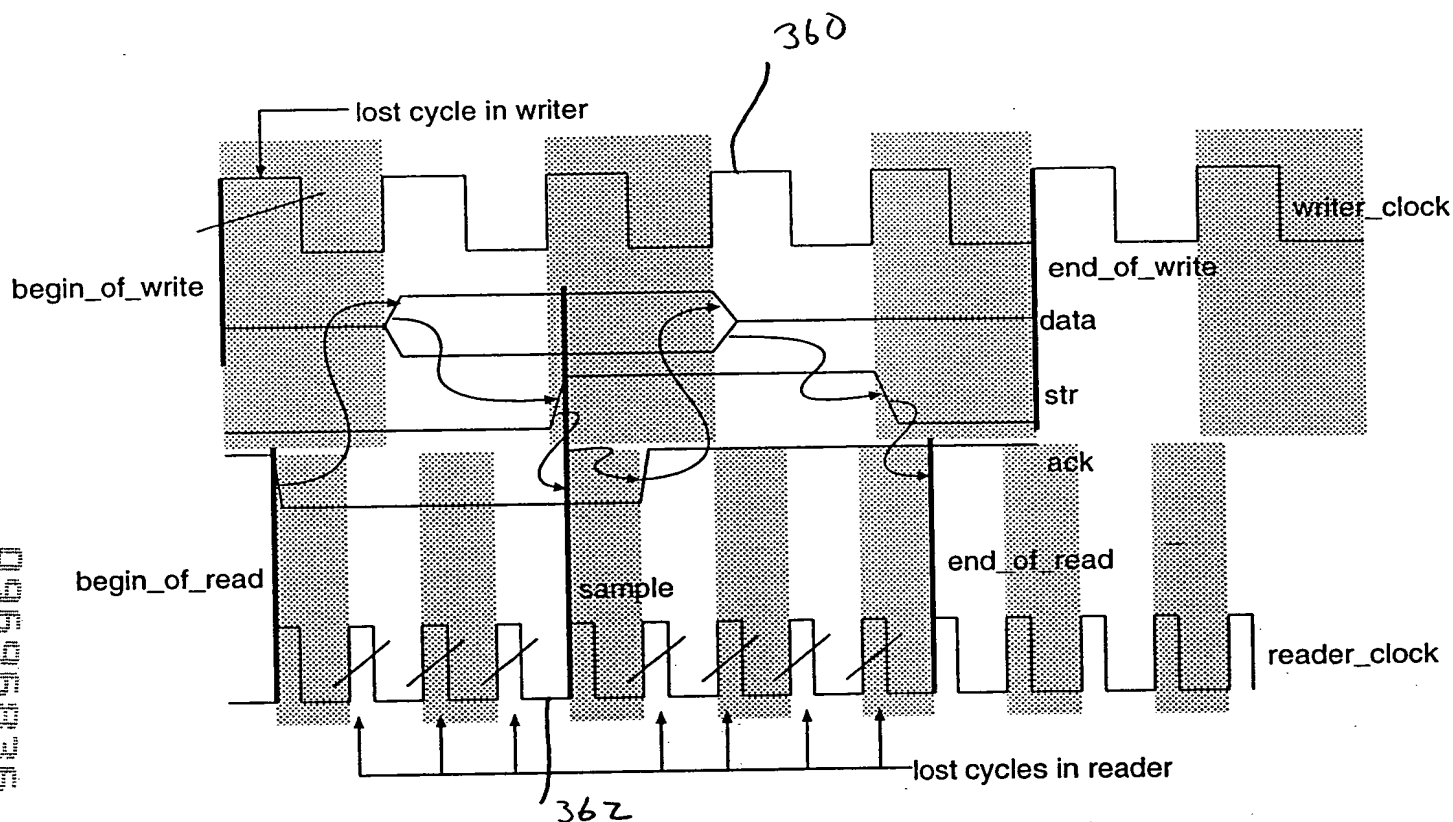


Figure 14.

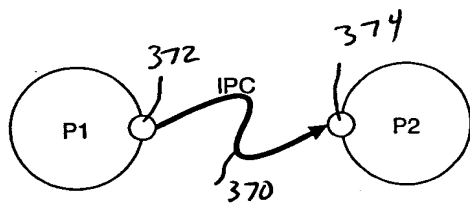


FIG. 15A

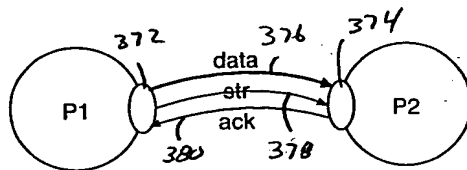


FIG. 15B

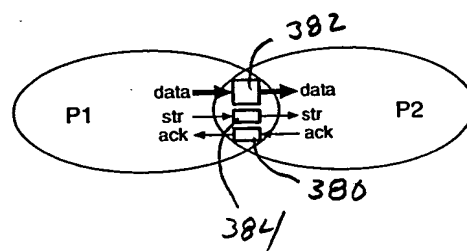


FIG. 15C

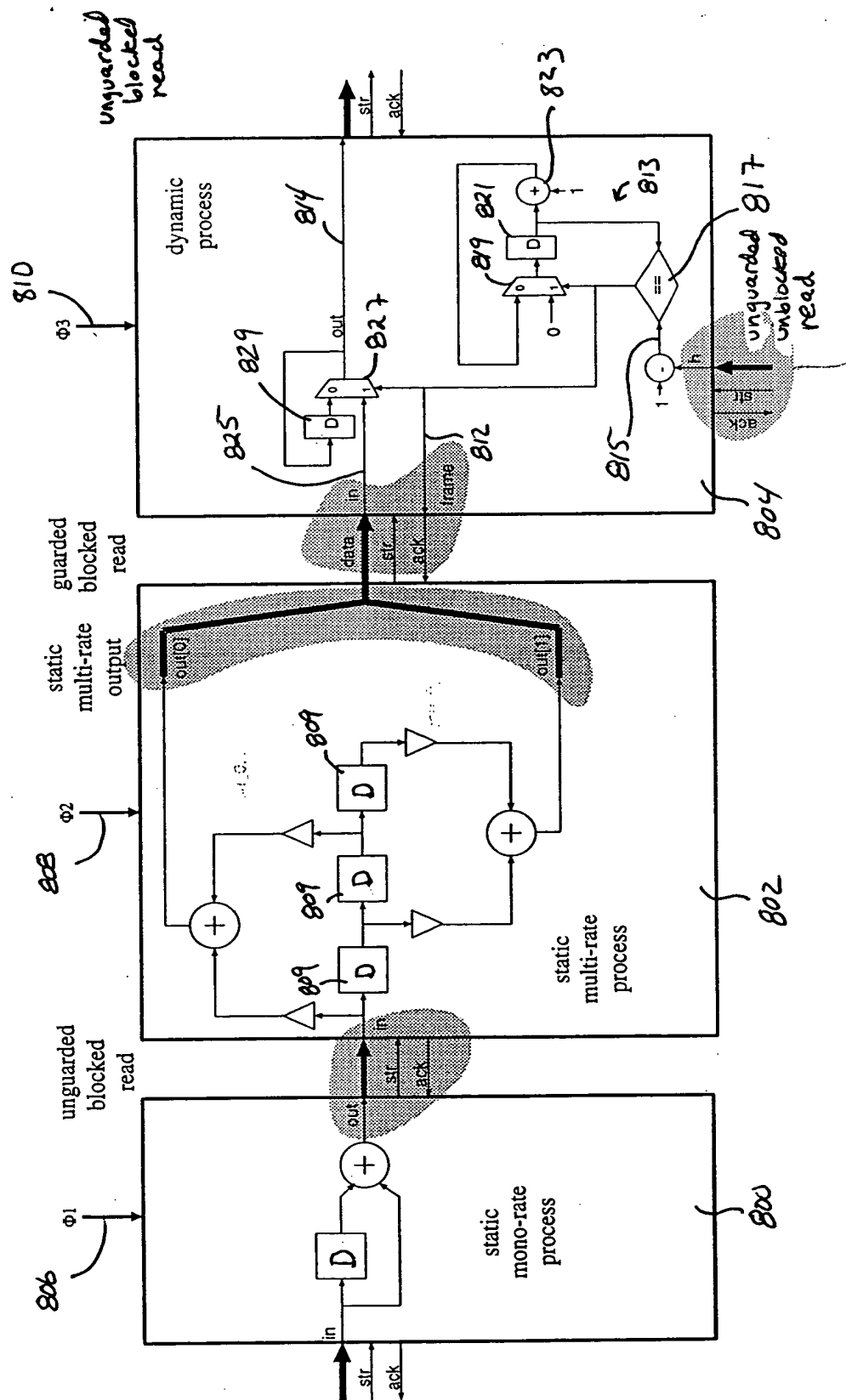


Figure 16

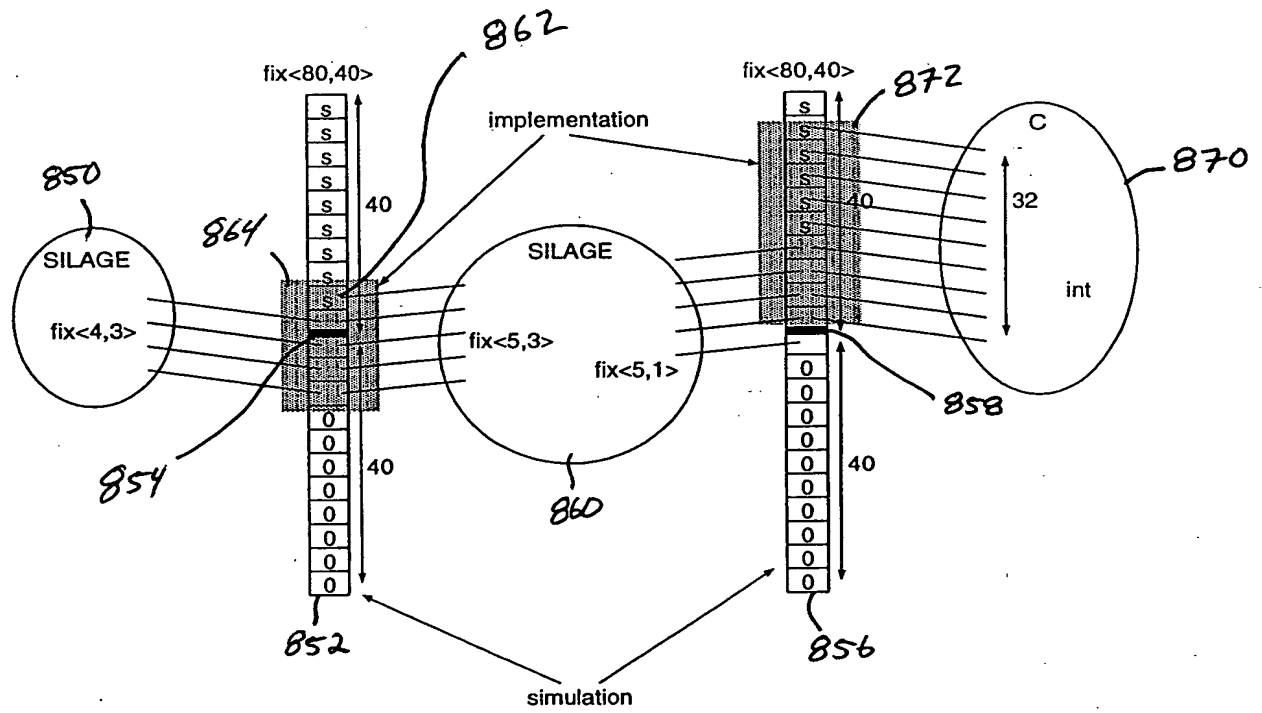


Figure 17: C...

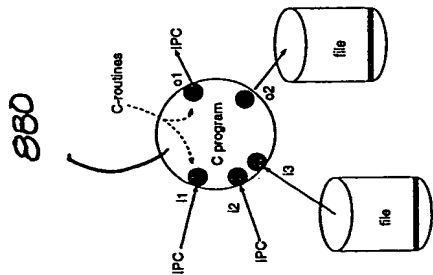


FIG. 18A

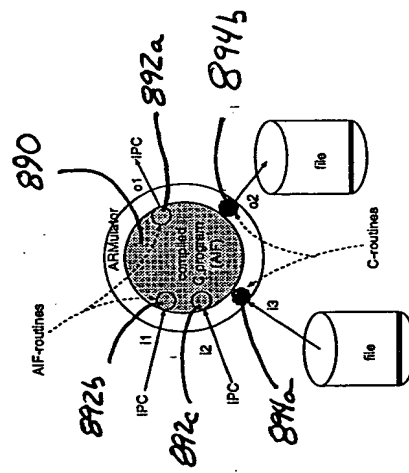


FIG. 18B

IPC

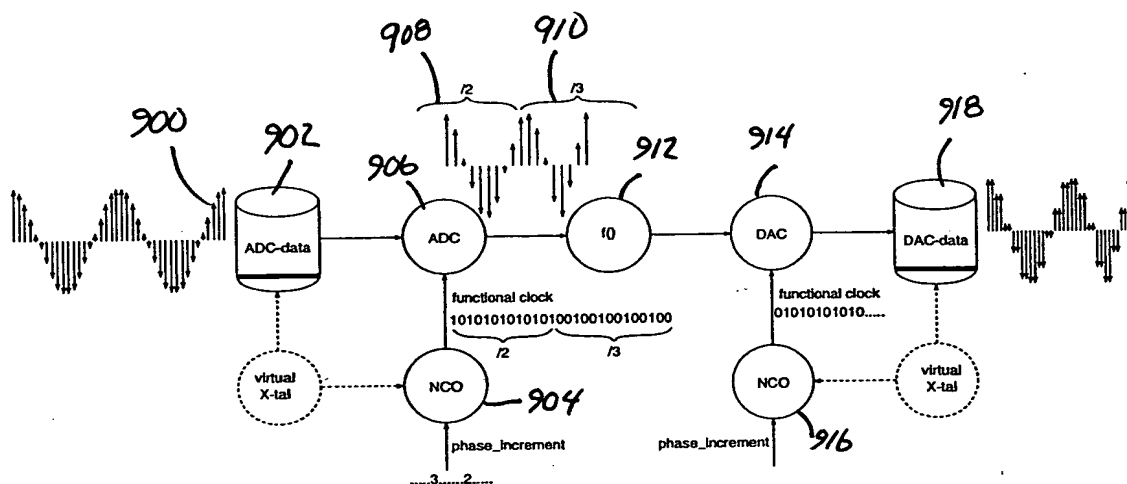


Figure 19.

00520T" 9E896960

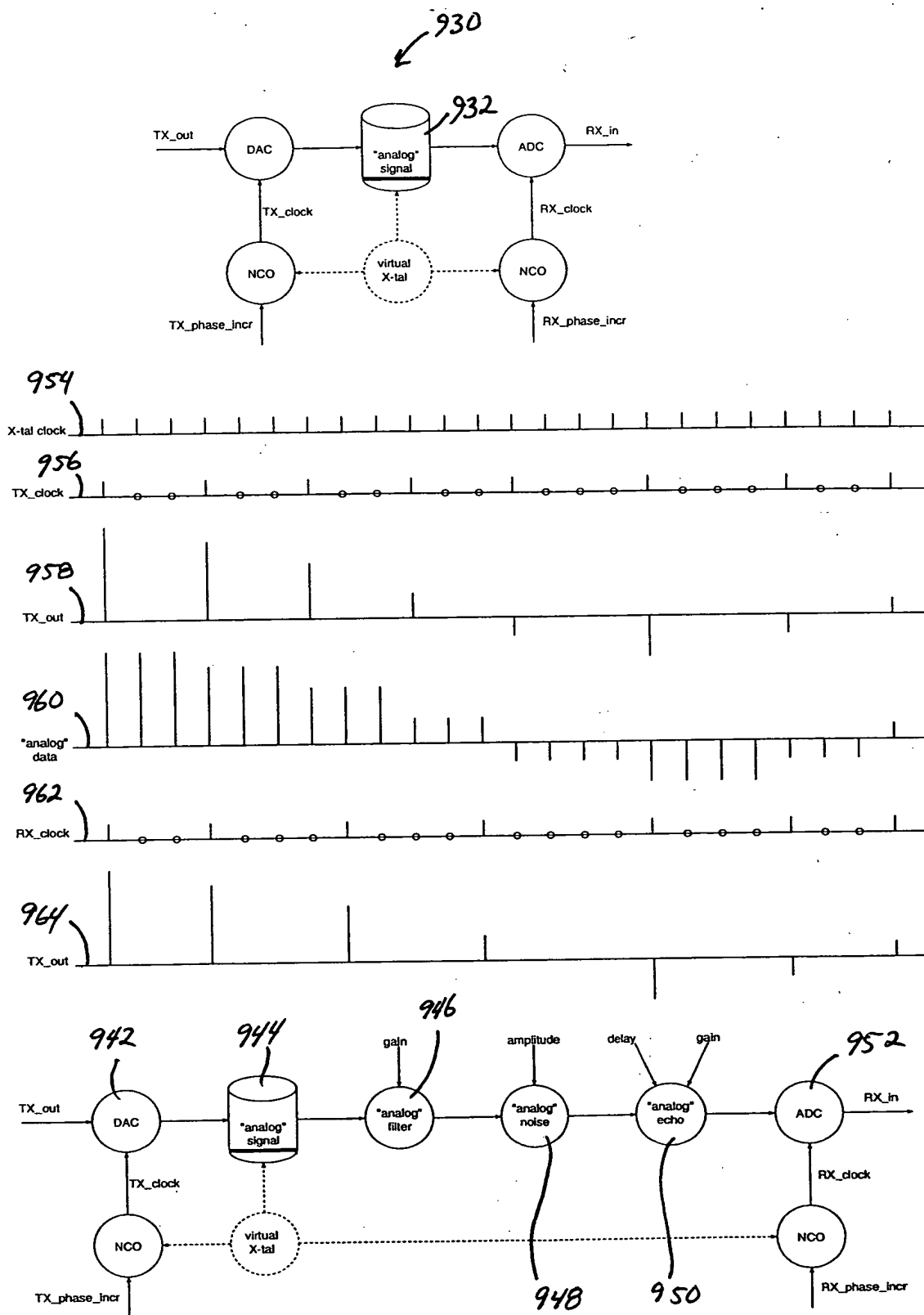


Figure 20:

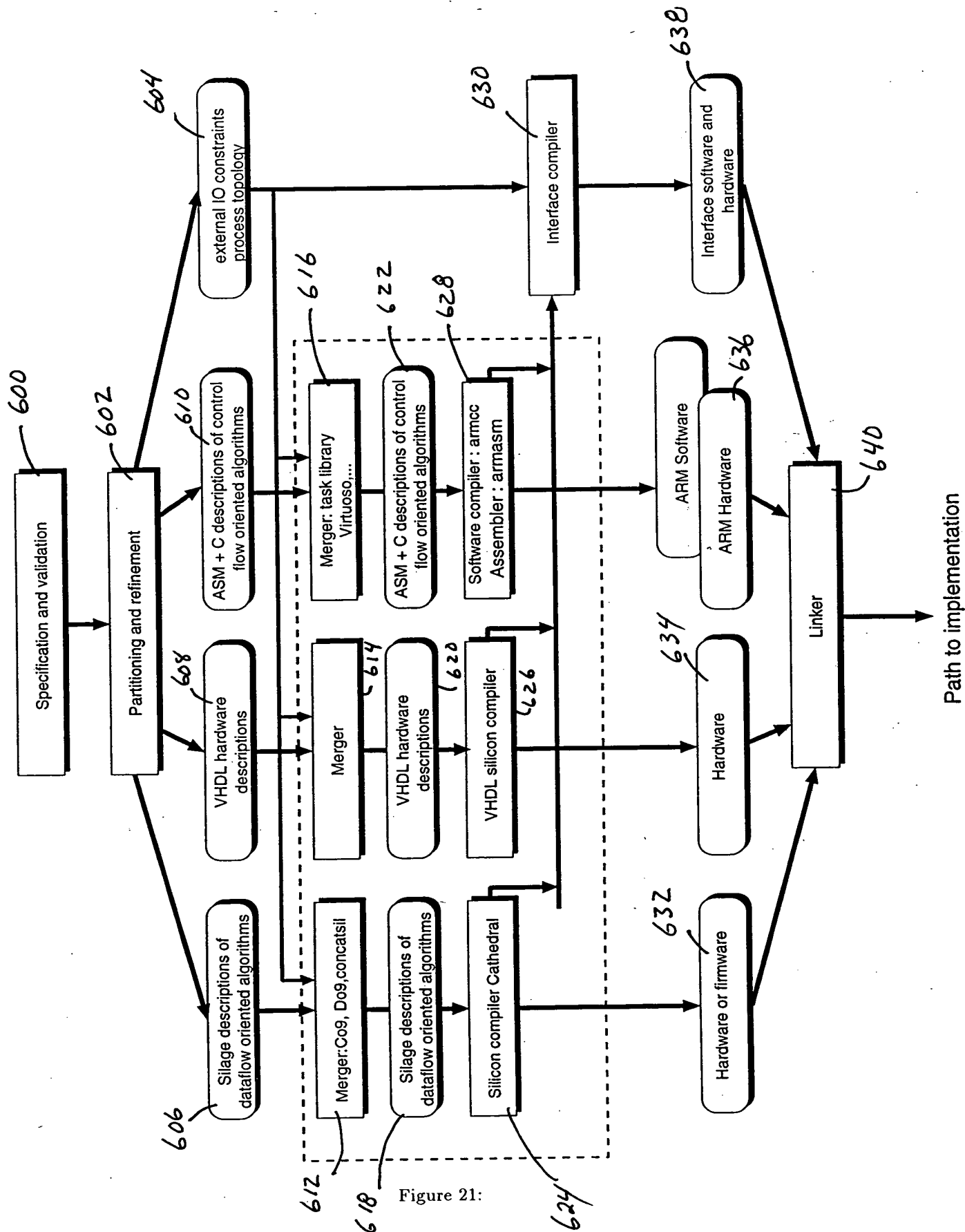


Figure 21:

00520T" 9E896960

1000a

1020a

1030a

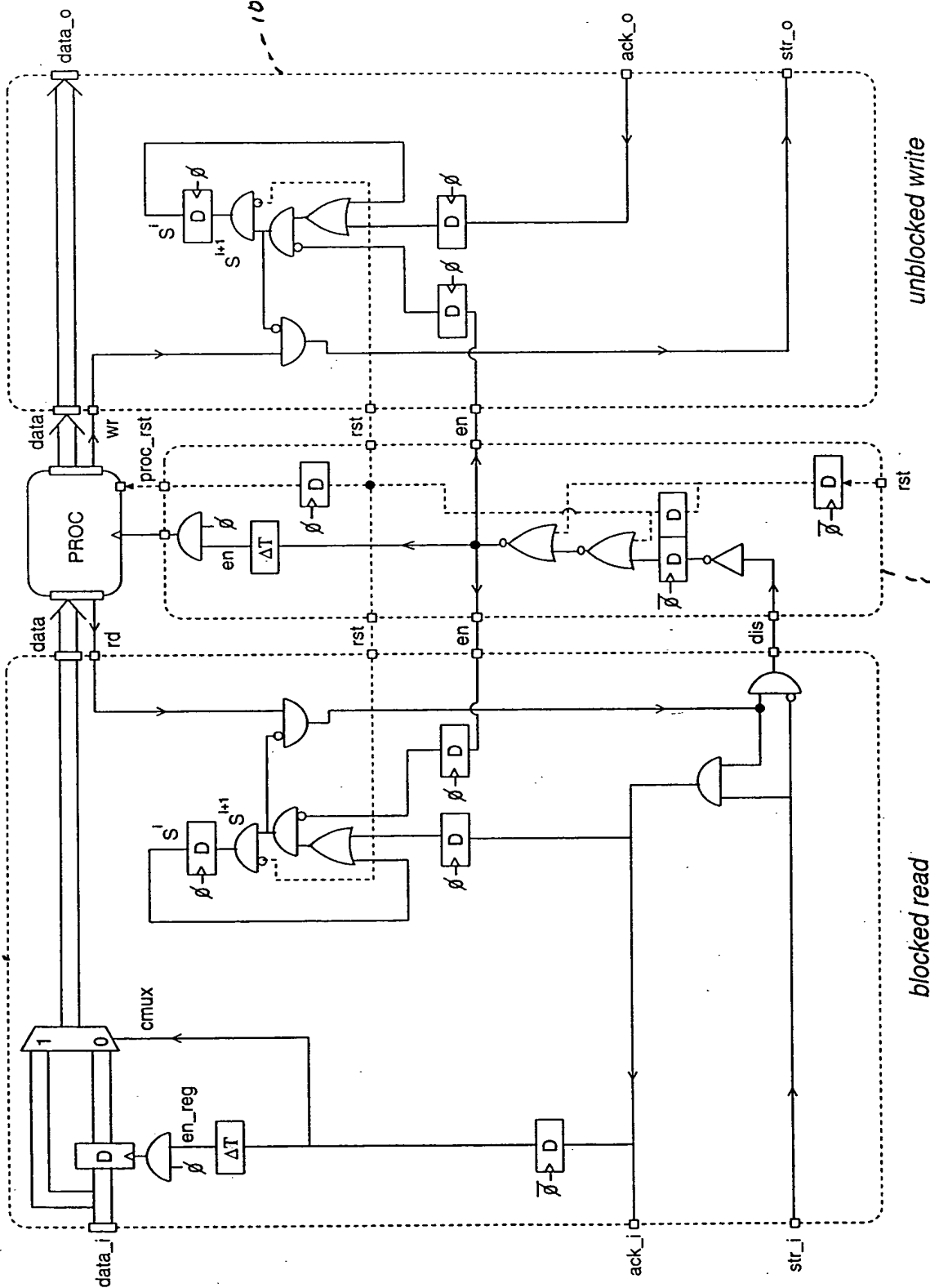


Figure 23

00520T" 9E896960

1000b

1020b

1030b

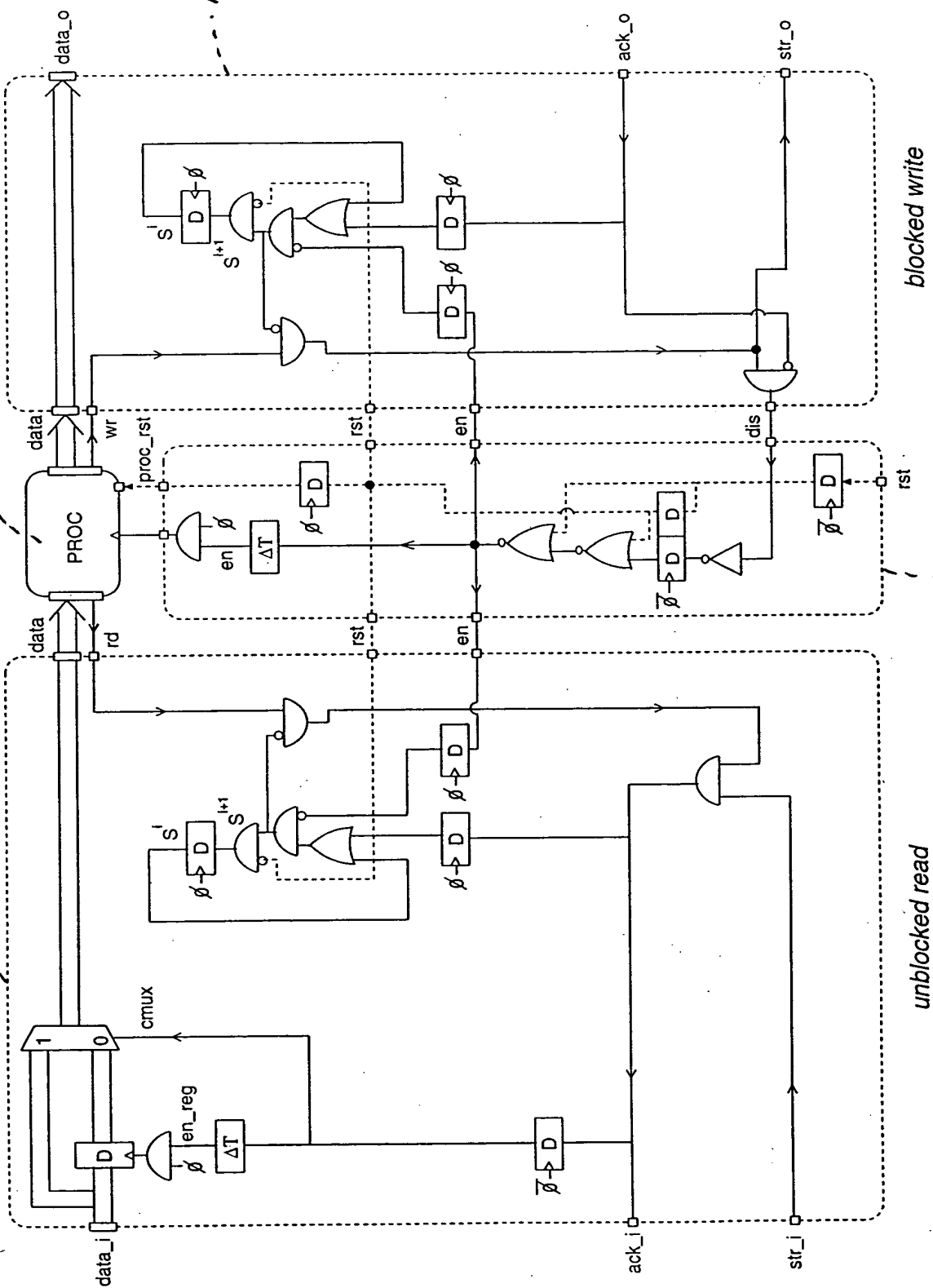


Figure 24

005201" 9E896960

10201

unblocked write

unblocked read

10301

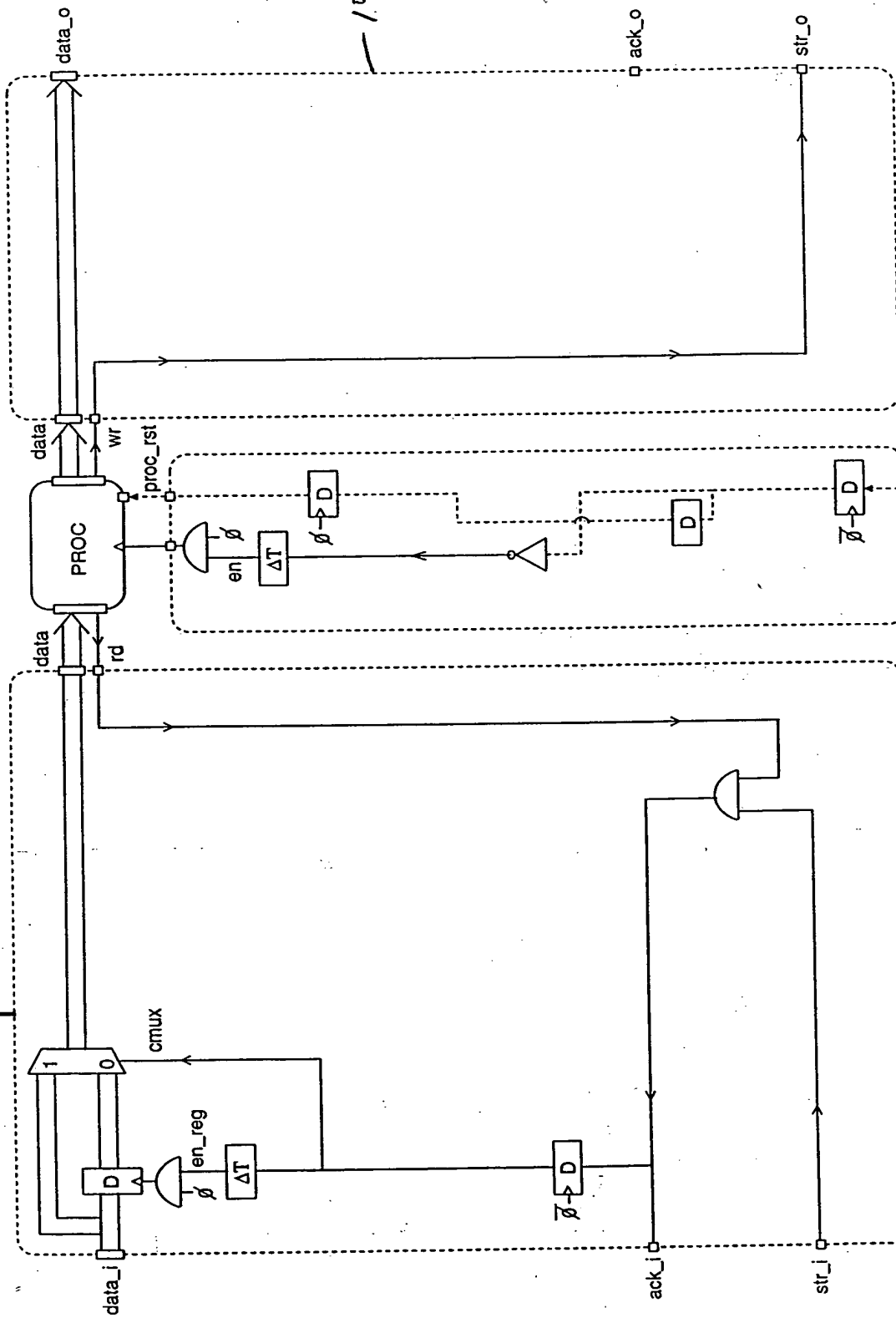


Figure 25:

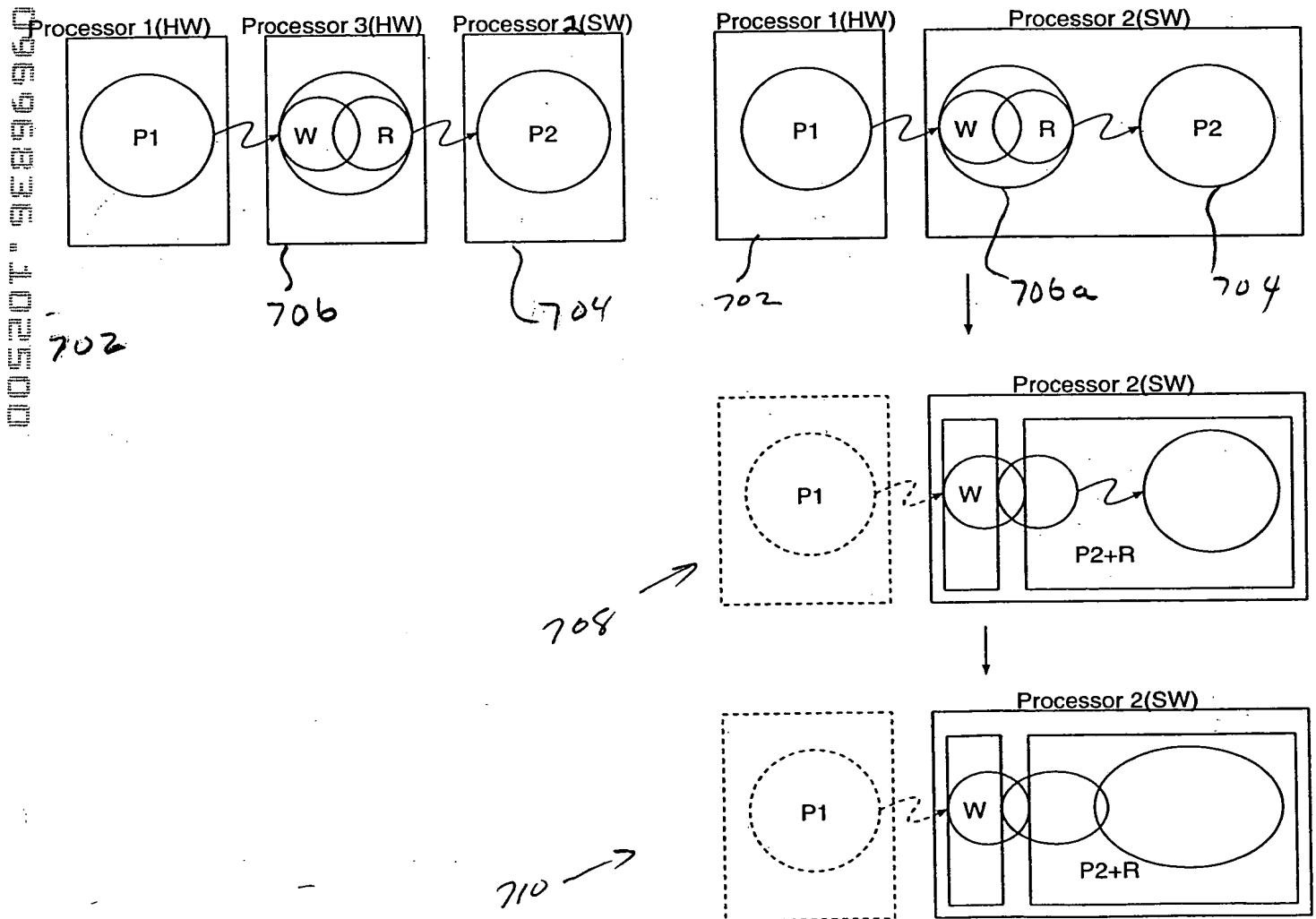


Figure 26: Refinement of a FIFO channel.

005207" 9889960

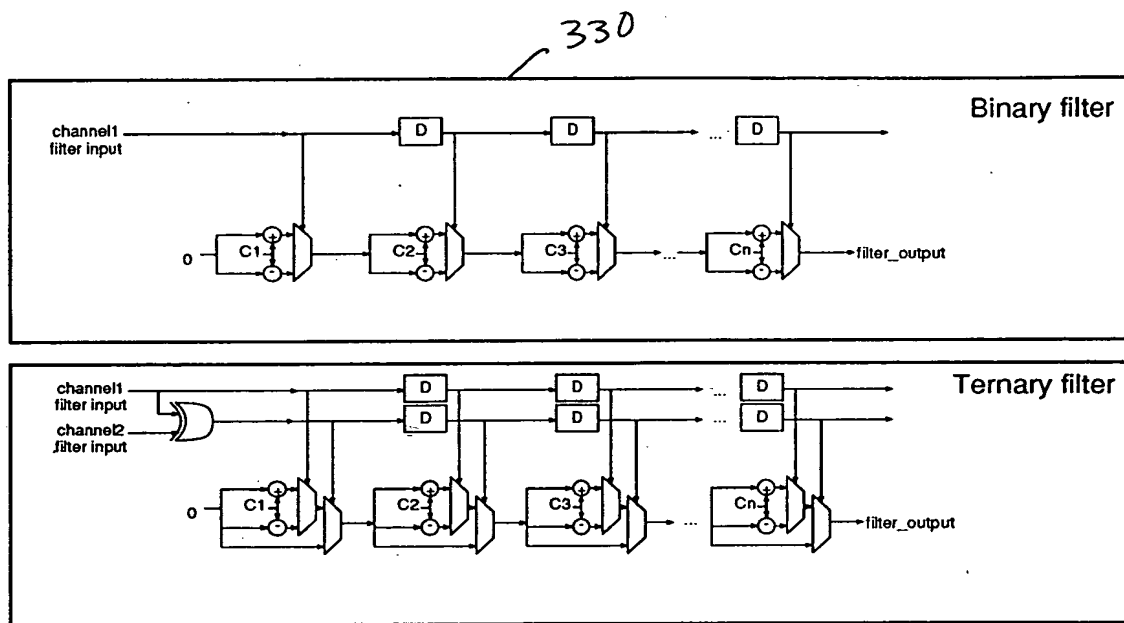


Figure 27

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